REMARKS/ARGUMENTS

Claims 1, 3-9, 11, and 13-18 are pending in this application, of which claims 1 and 13 are independent. By way of this amendment, claims 1, 3-9, 11, and 13-18 are amended and claims 2, 10, and 12 are canceled.

OBJECTION TO THE DRAWINGS

In section 4 on page 2, the Office Action objects to the drawings under 37 C.F.R. § 1.83(a) for allegedly failing to show the subject matter of claims 6-8 and 15-16.

Claims 6 and 15 recite that a latch being held open changes over time, while claims 7 and 16 recite a first and second latch being held open for different lengths of time and claim 8 recites varying the length of time the system operates in reduced mode. FIG. 3 of the application illustrates an exemplary enable signal for a latch, along with two varying "safe" control signals to use with a latch and a fourth "unsafe" signal to avoid using with the invention. As supported by paragraphs [0042]-[0043] of the published version of the specification, the control signal determines when a latch is in reduced mode by specifically controlling when a latch is held open.

Accordingly, Applicant hereby amends Figure 3 to better illustrate the subject matter of the claims. In particular, Applicant has amended Figure 3 to more clearly illustrate the varying enable and control signals, showing the control signals holding open the different latches at different times and for different lengths

of time, along with a varying length of time the system operates in reduced mode. Accordingly, Applicant respectfully requests that the objection to the drawings be withdrawn.

OBJECTION TO THE SPECIFICATION

In section 7 on page 3, the Office Action objects to the title of the Application for not being descriptive. The Office Action suggests the new title, "Method for reducing current peak in an asynchronous processor." Applicant thanks Examiner Petranek for this suggestion and hereby amends the title to the suggested title. Accordingly, Applicant respectfully requests that the objection to the specification be withdrawn.

CLAIM OBJECTIONS

In section 9 on page 3, the Office Action objects to claims 1-18 due to a number of informalities. Applicant thanks Examiner Petranek for pointing out these errors and hereby amends claims 1-18 to correct these errors. Accordingly, Applicant respectfully requests that the objection to claims 1-18 be withdrawn.

DOUBLE PATENTING

In section 24 on page 5, the Office Action provisionally rejects claims 1, 2, and 13 for alleged non-statutory obviousness-type double patenting as being unpatentable over claims 1-2 of co-pending application 10/598,583 to Bink et al.

(hereinafter, "the '583 application"). In section 25 on page 6, the Office Action rejects claims 1-18 for alleged nonstatutory obviousness-type double patenting as being unpatentable over U.S. Patent No. 7,423,449 to Bink et al. (hereinafter "the '449 patent") in view of "Computer Organization and Design: The Hardware/Software Interface" by Hennessy et al. (hereinafter Hennessy) and further in view of U.S. Patent No. 5,604,878 to Colwell et al. (hereinafter Colwell). In section 26, the Office Action provisionally rejects claims 3-12 and 14-18 for alleged non-statutory obviousness-type double patenting as being unpatentable over the '583 application in view of Hennessy and further in view of Colwell.

Applicant has filed terminal disclaimers herewith, complying with 37 C.F.R. § 1.321. Accordingly, applicant respectfully requests that the provisional rejection of claims 1-12 and 14-18 and the rejection of claims 1-18 for non-statutory obviousness-type double patenting be withdrawn.

REJECTIONS UNDER 35 U.S.C. § 112

In section 28 on page 7, the Office Action rejects claims 8, 10-12, and 18 under 35 U.S.C. § 112, ¶ 2, for allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

More specifically, claims 10 and 12 recite the limitations "the latch control circuits" and "each latch control circuit," and it is alleged that there is insufficient antecedent basis for such a limitation. Claim 10 also recites the limitation, "the

mode of operation," and it is alleged that there is insufficient antecedent basis for such a limitation. Claim 11 is rejected due to its dependency. Claims 8 and 18 both recite the limitation "the length of time," and it is alleged that there is insufficient antecedent basis for such a limitation.

Claims 8, 10-12, and 18 have been amended to resolve each antecedent basis issue. Accordingly, Applicant respectfully requests that the rejection of claims 8, 10-12, and 18 under 35 U.S.C. § 112, ¶ 2, be withdrawn.

REJECTIONS UNDER 35 U.S.C. § 103

In section 33 on page 9, the Office Action rejects claims 1-18 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Hennessy in view of Colwell. Applicant respectfully traverses these rejections.

Independent claim 1, as amended, recites:

> An electronic circuit comprising:
> first and second pipeline stages;
> a first latch positioned between the first and second pipeline stages; and
> a first latch control circuit connected to the first latch, said latch control circuit to receive a first control signal, said first control signal being randomly-generated and indicating the mode of operation of the electronic circuit;
> wherein the electronic circuit is adapted to operate in a normal mode in which the first latch is opened and closed in response to an enable signal controlled by the first latch control circuit, and a reduced mode in which the first latch is held open by the first latch control circuit.

Independent claim 13 contains a similar recitation. This subject matter finds support in paragraphs [0032]-[0038] of the published version of the specification. In

particular, the specification discloses a system and method of cryptography protection in a storage system by masking current spikes.

In an asynchronous pipeline, the system acts in normal mode for certain periods, while acting in reduced mode – where latches are unnecessarily held open – for varying periods to mask the current spikes associated with the change in the value of data passed through the pipeline. *See ¶¶ [0032]-[0033].* For a specific latch, the associated latch control circuit takes an incoming control signal and either allows the enable signal – the signal used in normal mode – to control the latch, or the latch is held open by allowing the supply voltage to hold the latch open until the control signal allows the latch to operate in normal mode and the enable switch closes the latch. *See Fig. 2; ¶¶ [0036]-[0038].*

Hennessy fails to disclose, teach, or suggest, "a first latch control circuit connected to the first latch, said latch control circuit to receive a first control signal, said first control signal being randomly-generated and indicating the mode of operation of the electronic circuit," as quoted and described above. In particular, Hennessy discloses a pipelined architecture with the capability of extending control through the pipeline system. *See pgs. 466-469; Fig. 6.25.* Hennessy specifically discloses synchronous pipeline architecture, with instructions passing through various stages of registers in a pipeline with each clock period. *See Figs. 6.32-6.33.*

Colwell similarly fails to disclose, teach, or suggest "a first latch control circuit connected to the first latch, said latch control circuit to receive a first control signal, said first control signal being randomly-generated and indicating the mode

of operation of the electronic circuit" (emphasis added). Rather, Colwell describes the operation of control logic with a multiplexer during a writeback conflict. The Colwell specification discloses a control circuit in a synchronous pipeline to control the length of the floating add point unit. *See col. 7, lns. 55-56.* The control logic controls a multiplexer, which chooses between the third pipe stage in normal mode, and the previous clock cycle's buffered result from the pipeline extending buffer when the control logic determines that a writeback conflict will exist. *See col. 7, lns. 60-66.*

As mentioned in the Office Action, "[t]he combination [of Hennessy and Colwell] uses elements 61-62 to bypass the MEM/WB pipeline register by keeping the pipeline register open when a writeback contention will be avoided. The control signal is the signal from element 62 that allows two pipeline stages to affectively [sic] become a single stage." The Office Action asserts that:

> The advantage of bypassing an extra pipeline stage that isn't needed for instructions is that these instructions will be allowed to *retire earlier and result in increased performance when there is no writeback contention* (Colwell: Column 2 lines 65-67 continued to column 3 lines 1-9). One of ordinary skill in the art would have been motivated to modify Hennessy to perform the pipeline stage bypassing of Colwell into the processor for the advantage of increasing performance of the processor of Hennessy. (Emphasis added)

Applicant respectfully disagrees with this assertion. Hennessy in view of Colwell fails to teach, disclose, or suggest, "a first latch control circuit connected to the first latch, said latch control circuit to receive a first control signal, said first control signal being randomly-generated and indicating the mode of operation of the

electronic circuit," as recited in claim 1 and similarly recited in claim 13. As discussed above, the claimed latch control circuit receives an independent signal that is randomly-generated for the purpose of hiding current peaks in the associated latches. This varies significantly from the combination of Hennessy and Colwell, which fails to disclose an independent, randomly-generated signal to control when a latch is held open. Hennessy and Colwell, therefore do not disclose, teach, or suggest all of the above-recited subject matter.

Accordingly, Applicant respectfully submits that independent claims 1 and 13 be allowed. Claims 3-9 and 11 depend on independent claim 1 and claims 14-18 depend on independent claim 13, respectively, and are allowable at least based upon these dependencies. By way of this Amendment, claims 2, 10, and 12 are canceled. Accordingly, Applicant respectfully requests that the rejection of claims 1-18 under 35 U.S.C. § 103(a) be withdrawn.

CONCLUSION

In view of the remarks above, Applicant believes that each of the rejections/objections has been overcome and the application is in condition for allowance. In the event that the fees submitted prove to be insufficient in connection with the filing of this paper, please charge our Deposit Account Number 50-0578 and please credit any excess fees to such Deposit Account.

Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the attorney overseeing the application file, Aaron Waxler, of NXP Corporation at (408) 474-5256.

Respectfully submitted,
KRAMER & AMADO, P.C.

Date: July 31, 2009

Terry W. Kramer
Registration No.: 41,541

Please direct all correspondence to:
Corporate Patent Counsel
NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131
CUSTOMER NO.: 65913